Zero-Sequence Voltage Elimination for Dual Fed Common dc-link Open-End Winding PMSM High Speed Starter-Generator, Part II: Dead Time Hysteresis Control of Zero-Sequence Current

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***Abstract*—In a common dc link dual-fed Open-End Winding Permanent Magnet Synchronous Motor (OEW-PMSM) topology it is well known how the additional flow of a Zero-Sequence Current (ZSC) is permitted. The low Zero-Sequence Impedance (ZSI) characteristic of high speed machines leads to high intensity and high frequency ripple of the ZSC. Therefore there is the necessity to eliminate the Zero-Sequence-Voltage (ZSV) produced by the two Voltage Source Converters (VSCs) that feed the machine. Furthermore the non-sinusoidal back Electro Magnetic Force (back EMF) causes the circulation of a third harmonic ZSC. An OEW-PMSM high speed starter-generator fed by a dual-inverter with single dc link is considered. Part I of this work proposes a modulation for the considered topology able to eliminate instantaneously the ZSV produced. In this paper a detailed analysis of the Dead Time (DT) effect on the ZSV has been carried out and a novel hysteresis control for the ZSC using the DT as a control action is presented. The DT produces a ZSV distortion on the zero-axis that can be used to control the third harmonic ZSC flowing due to the non-sinusoidal machine back EMF.**

***Index Terms*—Open-End Winding Machine, Permanent Magnet Synchronous Motor, Dual-Fed Single dc-link drive, Dead Time, Zero-Sequence Voltage, Zero-Sequence Current, Histeresys Control.**

I. Introduction

One dc supply and a floating bridge [1], two isolated dc power supplies [2] or a single dc supply can be adopted for the dual-fed OEW. The causes of circulation of additional ZSC can be attributed to ZSV generated by the converters, third harmonic component of the back EMF, devices' DTs and voltage drops as widely discussed in [3], [4]. The single dc link topology allows for a significant simplification of the OEW drive but at the same time it allows the ZSC to flow freely in the system [5]. In particular conditions such as extremely low ZSI the high-frequency ZSV produced by the modulation cannot be neglected since the low ZSI will not filter out anymore these frequencies. This paper considers the case of an high speed OEW-PMSM, therefore characterized by low phase inductance ($355\mu H$). The ZSV must be instantaneously zero, in order to avoid the circulation high intensity ZSC. The PMSM considered in previous works [6] [4] [7] have significantly higher phase inductances (respectively $8.5mH$, $61.7mH$ and $17mH$) compared to the high speed OEW here considered. As discussed in Part I, many modulations for the single dc link OEW-PMSM drive have been proposed aiming to control to zero the average ZSV produced by the two converters on the controller sampling time [6], [8]–[10].

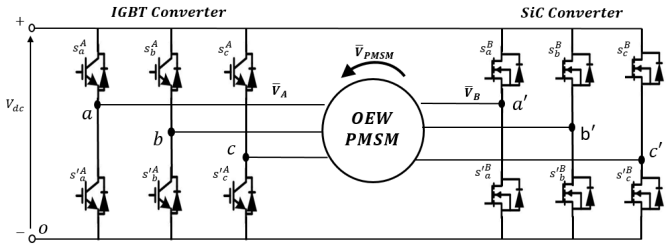

Fig. 1. Dual-Fed single dc-link OEW-PMSM with mixed technology VSCs.

These modulations previously proposed in the literature provide a controllable ZSV which is not instantaneously zero on the controller sampling time therefore causing an unacceptable ZSC if used to control a OEW-PMSM characterized by low ZSI. Furthermore the modulations existing in the literature are not suitable to control the mixed technology dual-inverter that has been selected to drive the high speed starter-generator. As demonstrated in [11], [12] SiC technology in combination with standard IGBT devices can be used to increase the system efficiency. The SVPWM proposed in Part I of this work achieves instantaneous elimination of the ZSV applied by the two VSCs. The IGBT VSC is six-step modulated introducing intense harmonics which are compensated by the SiC-based VSC, which can be seen as an active filter. Due to the rotor shaping and coil arrangement most of the PMSM have a non-sinusoidal back EMF, mostly characterized by its third harmonic. As shown in Part I even if the ZSV applied by the VSCs is instantaneously eliminated the ZSC can still flow in the system due to the third harmonic back EMF. The solutions previously proposed to eliminate the ZSC are based on introducing a regulator on the zero-axis and then applying a modulation able to synthesize the reference ZSV. Different solutions have been proposed, a simple PI regulator for the zero-axis is proposed in [6], a Proportional Resonant (PR) controller is implemented in [4] where the reference ZSV is synthesized by zero vector redistribution while in [10] the ZSC is effectively eliminated with a frequency adaptive PR controller to take into account that the ZSC frequency changes according to the operating speed. Since a ZSV cannot be

applied to the OEW-PMSM characterized by low ZSI, it is necessary to find an alternative solution to eliminate the ZSC. Since a zero-axis control cannot be performed in the average sense the possibility to use the DTs as a control action has been evaluated. The effect of the DT on the ZSV has been analysed. In [13], [14] a detailed model of the inverter non-linearities is proposed. Techniques for feed-forward compensation of the DTs and voltage drops are proposed in [13], [15], [16]. These methods need an off-line identification of the inverter parameters while in [17] the identification is done at the start up by injecting a set of dc and ac currents. An alternative method to compensate the DT for the PWM based modulators is the Pulse Based Dead Time Compensation (PBDTC) method [18], which allows to identify when the ZSV distortion introduced by the DT happens and its polarity. In this paper the SVM for the mixed technology dual-inverter proposed in Part I is adapted to an hybrid SVPWM in order to use the PBDTC. In this way each ZSV distortion introduced by the DT time can either be compensated or not, in this way full control of the DT voltage distortion on each converter's leg is achieved. Given the high dynamics of the ZSC the zero-axis controller needs to be implemented in FPGA, the novel hysteresis control of the ZSC using the converter's ZSV distortion introduced by the DT as a control action is presented and experimentally validated. The hysteresis band can be selected as small as desired to eliminate the ZSC produced by the third harmonic back EMF of the machine. The focus of this work is to develop an alternative way to control the ZSC for the mixed technology dual-inverter selected to control the high speed starter generator OEW-PMSM drive.

II. Equivalent Zero-Sequence Circuit for the OEW-PMSM

A 3-phase, p-pole, PMSM [19] where the neutral point of the stator windings has been opened is considered. The mathematical system of equations describing the behaviour of the machine are reported in Part I. The dynamic behaviour of the zero-sequence axis for the OEW-PMSM is described by (1)

$$V_0^A - V_0^B = R_s i_0 + L_0 \frac{di_0}{dt} + 3\omega_e \lambda_m k_{3\lambda} cos(3\theta) \quad (1)$$

where V_0^A and V_0^B are generated by the VSCs and $3\omega_e \lambda_m k_{3\lambda} cos(3\theta)$ is generated by the third harmonic back EMF. ω_e is the machine electrical speed, L_0 is the 0-axes inductance and R_s is the stator windings resistance. Since a common dc-link topology has been chosen the zero-sequence circuit cannot be neglected, therefore the third harmonic back EMF has to be considered. λ_m is the peak flux linkage established by the rotor permanent magnets. $k_{3\lambda}$ is defined as the ratio between the third harmonic flux and λ_m. θ is the rotor angular position of the machine. It can be noticed that even if the ZSV $V_0^A - V_0^B$ produced by the dual-inverter is instantaneously eliminated ZSC would still flow due to the third harmonic back EMF.

TABLE I
Single Inverter Switching States

Voltage Vector	Gate Signals	V_α	V_β	V_0
V_0	[0 0 0]	0	0	$-1/2$
V_A	[1 0 0]	$2/3$	0	$-1/6$
V_B	[1 1 0]	$1/3$	$1/\sqrt{3}$	$1/6$
V_C	[0 1 0]	$-1/3$	$1/\sqrt{3}$	$-1/6$
V_D	[0 1 1]	$-2/3$	0	$1/6$
V_E	[0 0 1]	$-1/3$	$-1/\sqrt{3}$	$-1/6$
V_F	[1 0 1]	$1/3$	$-1/\sqrt{3}$	$1/6$
V_7	[1 1 1]	0	0	$1/2$

III. Dual-Fed OEW-PMSM Drive Reference Voltages

The two VSCs use different technologies for the power modules, IGBT and SiC devices respectively. As explained in Part I the voltage references for the two VSCs are chosen in order to exploit the different nature of the power devices used. The IGBT VSC is square wave modulated at the fundamental frequency set by the motor speed while the SiC converter supplies the voltages necessary to have sinusoidal voltages on the machine, therefore their references voltages are

$$\begin{cases} \overline{V}_A^{*SW} = \dfrac{V_{dc}}{2} sign(\overline{V}_{PMSM}^*) \\ \\ \overline{V}_B^* = \overline{V}_A^{*SW} - \overline{V}_{PMSM}^* \end{cases} \quad (2)$$

Where $\overline{V}_{PMSM}^*$ are the OEW-PMSM reference phase voltages obtained from standard Field Oriented Control (FOC). The voltage vectors admissible to synthesize the reference voltages (2) are the ones with zero V_0 component if the ZSV $V_0^A - V_0^B$ wants to be kept at zero. Table I shows the voltage components in the $\alpha\beta 0$ reference system for the 8 switching states for a single VSC. The active vectors of the single inverter can be grouped in two sets, the ones that produce a negative ZSV (V_A, V_C and V_E) and the ones that produce a positive ZSV (V_B, V_D and V_F). VSC B synthesizes its reference voltage according to which set belongs the active voltage vector that the square-wave modulated VSC A is applying. The dwelling times for the three active vectors can be found similarly as done for a standard SVM and are reported in Part I. The three vectors can therefore be applied in 3! = 6 possible permutations. The three vectors will be identified as t_{min}, t_{med} and t_{max} according to their dwelling time. Thanks to the modulation introduced the ZSV V_0^{PMSM} generated by the converters is instantaneously zero apart from the voltage distortion introduced by the DTs, therefore a ZSC PI controller is not needed.

IV. Dead-Time Effect on OEW-PMSM ZSV

Failure of the switching devices and even of the whole inverter is possible if a DT is not added in the control scheme to ensure proper operation of the inverter. In this way the bridge shoot through can always be avoided eliminating additional losses or even thermal runaway. Usually several micro seconds are required for the DT which are no longer ignorable in the inverter modelling. Even if the gate signal DT

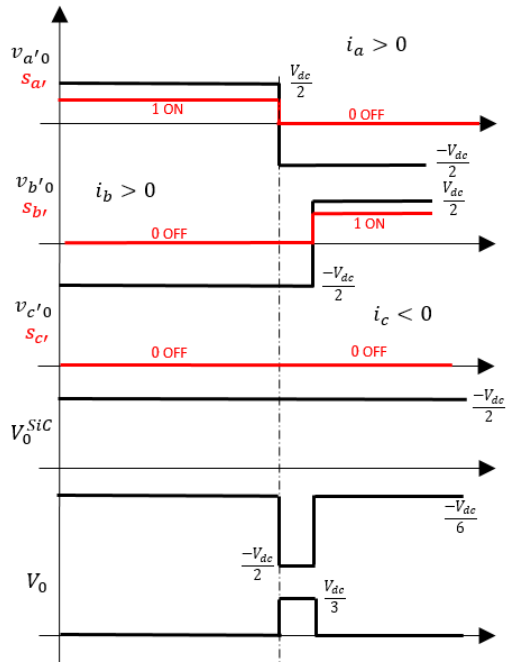

Fig. 2. DT effect on V_0^{PMSM}. From top: top gate signal of leg a of VSC B and relative voltage. top gate signal of leg b of VSC B and relative voltage. top gate signal of leg c of VSC B and relative voltage. ZSV V_0^B of VSC B and ZSV V_0^{PMSM} on the OEW-PMSM

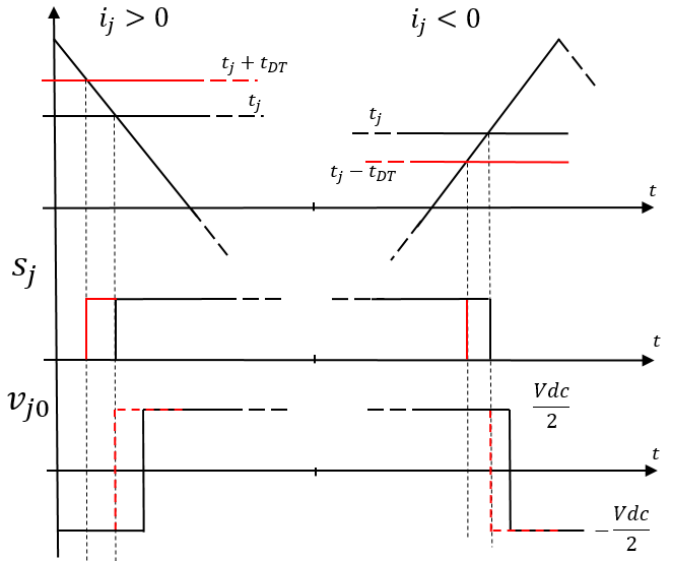

Fig. 3. PBDTC compensation technique. Top: triangular PWM carrier, refernce signal (black line) and compensated reference signal (red line). Middle: top j^{th} phase gate signal (black line) and top compensated gate signal (red line). Bottom: j^{th} phase leg voltage.

is always applied, the phase voltage distortion happens only in the two following cases: s_j switches from 0 to 1 and $i_j > 0$ or s_j switches from 1 to 0 and $i_j < 0$ where i is the phase current, s is the switching state of the leg top device and j stands for the j^{th} inverter leg. Fig. 2 shows the three states of VSC B and their output phase voltages $v_{a'0}, v_{b'0}$ and $v_{c'0}$ in the case of $i_a > 0, i_b > 0$ and $i_c < 0$. The set of vectors which produce a negative ZSV is considered, in particular the transition from V_A to V_C is analysed. Therefore the DT will cause a voltage distortion only on $v_{b'0}$. In fact when both the upper and lower devices are off the phase current will keep flowing through the lower diode keeping the voltage clamped to $-\frac{V_{dc}}{2}$. During the DT the ZSV V_0^A is $-\frac{V_{dc}}{2}$ different from the ZSV produced by VSC A which is $-\frac{V_{dc}}{6}$. The result is a positive ZSV V_0 on the machine that will cause a ZSC to circulate. It can be noticed that for the same switching V_A to V_C with $i_a < 0, i_b < 0$ and $i_c > 0$ that the DT distortion on leg a' due to a transition from 1 to 0 causes a negative ZSV on the machine. Similarly the same analysis can be done for the set of vectors $t_{V_B}, t_{V_D}, t_{V_F}$ which produce a positive ZSV observing the same behaviour as the vectors $t_{V_A}, t_{V_C}, t_{V_E}$.

A. Dead-Time compensation for PWM Voltage Inverter

The Pulse-Based DT Compensation (PBDTC) is a simple but efficient method for PWM VSC proposed in [18] to compensate for the voltage distortion introduced by the DT. The two switching conditions that lead to a voltage distortion are shown in Fig. 3. The compensation technique is based on being able to identify the switching condition for which there is distortion. Firstly the sign of the i_j phase current is checked, secondly the value of the top gate signal s_j at the previous

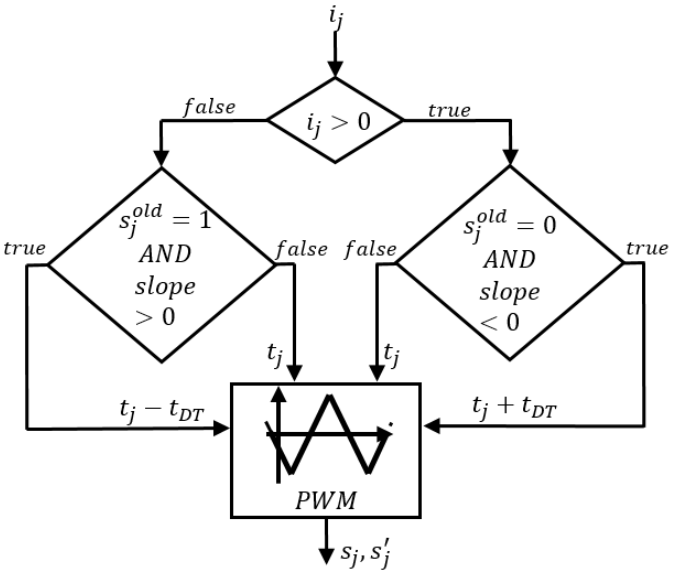

Fig. 4. PBDTC block diagram.

time instant and the carrier slope are checked. In fact if s_j is 1 and the carrier slope is positive it means there will be a transition from 0 to 1, vice versa if s_j is 0 and the carrier slope is negative the commutation will be from 1 to 0, the leg switch will be affected by voltage distortion depending on the phase current sign according to Fig. 3. By lowering or rising the leg's duty cycle of t_{DT} the gate's switch is anticipated of t_{DT} therefore obtaining the leg voltage to change at the ideal switching instant avoiding any voltage distortion. Fig. 4 reports the block diagram for the PBDTC.

B. Dead-Time compensation for the 3 active vectors SVPWM

In order to apply the PBDTC method to the SVM used to synthesize VSC B reference voltages $\overline{V}_B^*$ it is necessary to use an hybrid SVPWM technique. For each inverter leg a carrier based modulator which allows to apply only active voltage vectors is proposed. Each carrier starts at each sample time T_s from the value T_s and decreases with slope -1 so that it would reach zero for T_s. Referring to the modulation presented in Part I let's consider first the set of vectors which give a negative ZSV, once the dwelling time for $t_{V_A}, t_{V_C}, t_{V_E}$ are calculated they are reorganized in ascending order as t_{min}, t_{med} and t_{max}, from Table II the corresponding permutation of the order in which the three vectors are applied can be selected. The associated duty cycles can easily be found by observing the order in which the legs switch and the time for which each vector is applied. Fig. 5 shows the case where the permutation number 5 of the negative ZSV set is considered. The vectors t_{V_A}, t_{V_C} and t_{V_E} will be applied for t_{min}, t_{med} and t_{max} respectively. From the comparison of the leg carrier with the leg duty the leg gate signal is obtained. The time instants where the leg counters change slope can be pre-calculated according to the value of the dwelling times t_{min}, t_{med} and t_{max}. E.g. referring always to Fig. 5 and considering the leg $a^{'}$ the point at which the carrier changes slope from negative to positive is $t^1_{a'inf}$ that is $T_s - \frac{t_{min}}{2}$, the point $t^1_{a'sup}$ at which the carrier changes slope from positive to negative is $T_s + \frac{t_{med}+t_{max}}{2}$. Fig. 6 shows the legs' carriers, the legs' duties cycles and the corresponding gate signals for the permutation number 5 of the set of vectors which give a positive ZSV. Similarly as done for the other set the legs' duties are reported in Table III. With the proposed legs' carriers a PWM able to apply only the active vectors calculated from the 3 active vectors SVM is obtained. Furthermore the PBDTC method can now be applied as it would have been done for a standard PWM. After detecting if the voltage distortion due to the DT would take place, by simply rising or lowering the leg's duty cycle it is possible to anticipate the commutation and obtain the desired leg voltage and compensate the ZSV distortion that the DT would have caused.

C. Dead-Time Hysteresis Control of ZSC

Even if the VSCs' ZSV is set to zero thanks to the modulation proposed in Part I and the DT ZSV distortion is eliminated by the compensation proposed in Section IV-B, from (1) it can be seen that the ZSC would still not be zero due to the third harmonic back EMF of the machine. The ZSC i_0 is a sinusoidal waveform oscillating at three times the fundamental frequency of rotation. Due to the modulation implemented no ZSV can be applied on the OEW-PMSM therefore no control action is possible on the zero axis. Therefore also the possibility to use any standard controller to eliminate the ZSC cannot be considered since a variable ZSV to synthesize the reference ZSV coming from either a PI, a PR or a FAPR cannot be applied to the machine. In order to eliminate the ZSC the non-linear DT action is considered. The proposed DT compensation method allows to identify when the voltage distortion happens. It also allows to eliminate the

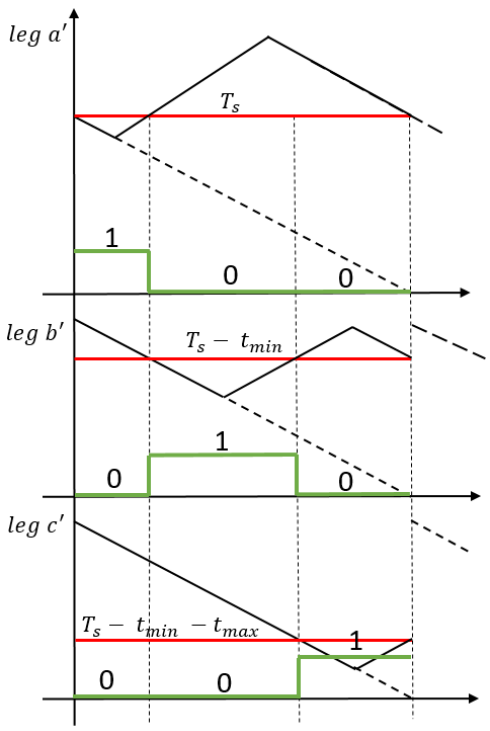

Fig. 5. Proposed SVPWM carriers (black line), modulating signals (red line) and gate signals (green line) for the set of vectors which give a negative ZSV.

TABLE II
PERMUTATIONS OF THE SET OF VOLTAGE VECTORS WHICH GIVE A NEGATIVE ZSV AND THEIR DUTY CYCLES FOR THE PROPOSED SVPWM.

Permutation	leg $\begin{bmatrix} a' \\ b' \\ c' \end{bmatrix}$: $t_{min}, t_{med}, t_{max}$	Duty Cycles
1	$\begin{bmatrix}0\\0\\1\end{bmatrix}, \begin{bmatrix}0\\1\\0\end{bmatrix}, \begin{bmatrix}1\\0\\0\end{bmatrix}$	$\begin{matrix}T_s - t_{min} - t_{med}\\ T_s - t_{min}\\ T_s\end{matrix}$
2	$\begin{bmatrix}0\\1\\0\end{bmatrix}, \begin{bmatrix}0\\0\\1\end{bmatrix}, \begin{bmatrix}1\\0\\0\end{bmatrix}$	$\begin{matrix}T_s - t_{min} - t_{med}\\ T_s\\ T_s - t_{min}\end{matrix}$
3	$\begin{bmatrix}0\\0\\1\end{bmatrix}, \begin{bmatrix}1\\0\\0\end{bmatrix}, \begin{bmatrix}0\\1\\0\end{bmatrix}$	$\begin{matrix}T_s - t_{min}\\ T_s - t_{min} - t_{med}\\ T_s\end{matrix}$
4	$\begin{bmatrix}1\\0\\0\end{bmatrix}, \begin{bmatrix}0\\0\\1\end{bmatrix}, \begin{bmatrix}0\\1\\0\end{bmatrix}$	$\begin{matrix}T_s\\ T_s - t_{min} - t_{med}\\ T_s - t_{min}\end{matrix}$
5	$\begin{bmatrix}1\\0\\0\end{bmatrix}, \begin{bmatrix}0\\1\\0\end{bmatrix}, \begin{bmatrix}0\\0\\1\end{bmatrix}$	$\begin{matrix}T_s\\ T_s - t_{min}\\ T_s - t_{min} - t_{med}\end{matrix}$
6	$\begin{bmatrix}0\\1\\0\end{bmatrix}, \begin{bmatrix}1\\0\\0\end{bmatrix}, \begin{bmatrix}0\\0\\1\end{bmatrix}$	$\begin{matrix}T_s - t_{min}\\ T_s\\ T_s - t_{min} - t_{med}\end{matrix}$

voltage distortion by anticipating of t_{DT} the switching time. Let's consider instead the case in which the ZSV distortion introduced by the DT is desired as a possible control action for the ZSC i_0. In fact the distortion introduced by the DT on the ZSV can be foreseen and it has a well known value as described in Section IV. Therefore the ZSV distortion can be used as a zero-axis control action for the third harmonic ZSC. As described in Section IV-A a commutation from 0

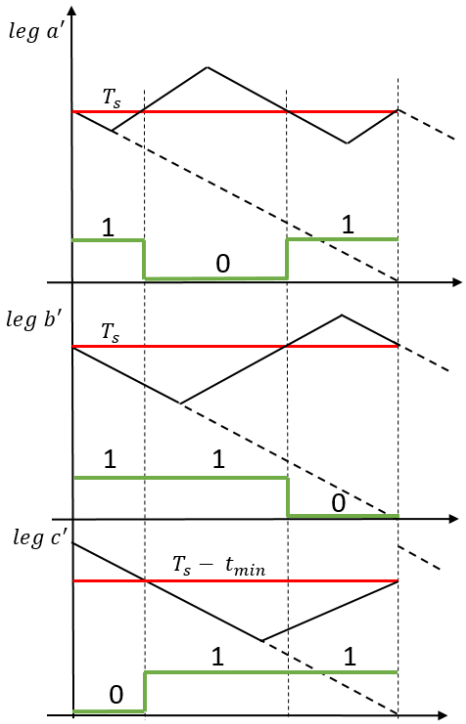

Fig. 6. Proposed SVPWM carriers (black line), modulating signals (red line) and gate signals (green line) for the set of vectors which give a positive ZSV.

TABLE III
PERMUTATIONS OF THE SET OF VOLTAGE VECTORS WHICH GIVE A NEGATIVE ZSV AND THEIR DUTY CYCLES FOR THE PROPOSED SVPWM.

Permutation	leg $\begin{bmatrix} a' \\ b' \\ c' \end{bmatrix}$: $t_{min}, t_{med}, t_{max}$	Duty Cycles
1	$\begin{bmatrix}1\\0\\1\end{bmatrix}\begin{bmatrix}0\\1\\1\end{bmatrix}\begin{bmatrix}1\\1\\0\end{bmatrix}$	$\begin{bmatrix}T_s\\T_s - t_{min}\\T_s\end{bmatrix}$
2	$\begin{bmatrix}0\\1\\1\end{bmatrix}\begin{bmatrix}1\\0\\1\end{bmatrix}\begin{bmatrix}1\\1\\0\end{bmatrix}$	$\begin{bmatrix}T_s - t_{min}\\T_s\\T_s\end{bmatrix}$
3	$\begin{bmatrix}1\\0\\1\end{bmatrix}\begin{bmatrix}1\\1\\0\end{bmatrix}\begin{bmatrix}0\\1\\1\end{bmatrix}$	$\begin{bmatrix}T_s\\T_s - t_{min}\\T_s\end{bmatrix}$
4	$\begin{bmatrix}1\\1\\0\end{bmatrix}\begin{bmatrix}1\\0\\1\end{bmatrix}\begin{bmatrix}0\\1\\1\end{bmatrix}$	$\begin{bmatrix}T_s\\T_s\\T_s - t_{min}\end{bmatrix}$
5	$\begin{bmatrix}1\\1\\0\end{bmatrix}\begin{bmatrix}0\\1\\1\end{bmatrix}\begin{bmatrix}1\\0\\1\end{bmatrix}$	$\begin{bmatrix}T_s\\T_s\\T_s - t_{min}\end{bmatrix}$
6	$\begin{bmatrix}0\\1\\1\end{bmatrix}\begin{bmatrix}1\\1\\0\end{bmatrix}\begin{bmatrix}1\\0\\1\end{bmatrix}$	$\begin{bmatrix}T_s - t_{min}\\T_s\\T_s\end{bmatrix}$

to 1 or from 1 to 0 could lead to a V_0 of $\frac{V_{DC}}{3}$ or $-\frac{V_{DC}}{3}$ respectively and thanks to the PBDTC method it is possible to identify when the DT distortion takes place and if it is a positive or negative ZSV. Based on the previous observation an hysteresis i_0 controller as been developed. Due to the high dynamics of the ZSC the controller cannot be implemented on the DSP microprocessor. The phase currents are sampled every 1 μs by the FPGA and used to calculate the ZSC. The

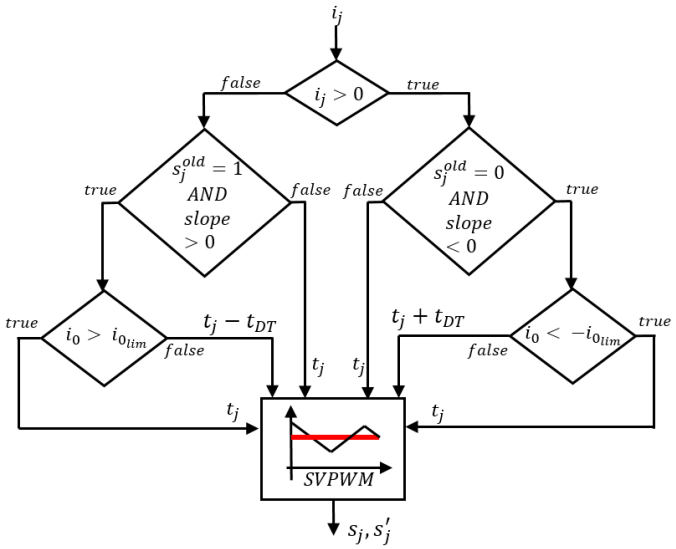

Fig. 7. Modified PBDTC logic for DT hysteresis control.

TABLE IV
HIGH SPEED STARTER-GENERATOR OEW-PMSM PARAMETERS.

L_q	355 [μH]	L_d	355 [μH]
R_s	1.64 [$m\Omega$]	p	3 [-]
λ_m	0.086532 [V s]	$k_{3\lambda}$	1.4110^{-3} [-]

FPGA implementation allows to calculate the i_0 current with high frequency and it can be checked if the i_0 current is bigger or smaller of the desired hysteresis band $[i_{0lim}, -i_{0lim}]$. If i_0 is higher than i_{0lim} the DT voltage distortion associated with a switch commutation from 1 to 0 which would lead to a V_0 of $-\frac{V_{DC}}{3}$ is not compensated. Instead a ZSV V_0 of $\frac{V_{DC}}{3}$ is applied when i_0 is lower than $-i_{0lim}$ by not compensating the DT distortion due to a device commutation from 0 to 1. At the beginning of each sample time which group of active vectors is applied is known, the DT happens at the transition from one voltage vector to the following. Whether the i_0 ZSC lays inside or outside the hysteresis band is added to identify if to compensate or not the DT. If the phase current is positive and a transition from 0 to 1 will happen than it means that a positive ZSV distortion will be introduced by the DT. If the ZSC is lower than the inferior limit of the hysteresis band than the ZSV distortion id desired and therefore it is not compensated by leaving the duty cycle to its original value of t_j. On the other hand if the ZSC is inside the hysteresis band then the duty cycle is corrected accordingly to compensate the DT ZSV distortion. The modified PBDTC logic is shown in Fig. 7. The DT hysteresis control, which allows for the ZSC elimination can be applied all over the range of operation of the dual-inverter drive with the proposed modulation. As shown in Part I it corresponds to the circle of radius V_{DC} in the $\alpha\beta$ plane. Furthermore it can be noticed that the DT hysteresis controller proposed does not depend on the OEW-PMSM parameters, it exclusively requires the knowledge of the VSC's DT.

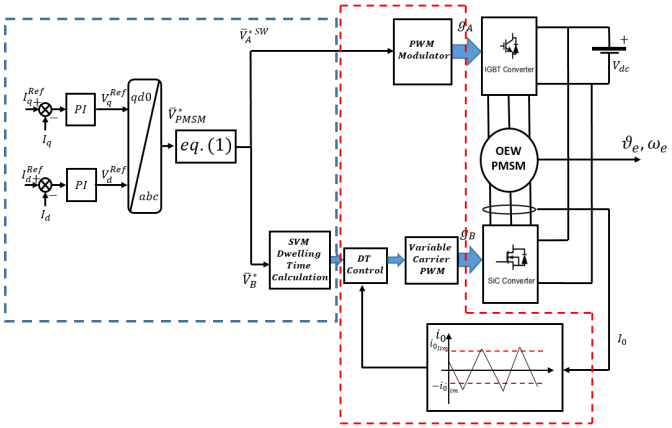

Fig. 8. Block scheme of the proposed control of the dual fed OEW-PMSM. DSP implemented controller in the dashed blue area and FPGA implemented controller in the red area.

TABLE V
OEW-PMSM UNDER TEST PARAMETERS

L_q	1.2 [mH]	L_d	1.2 [mH]
R_s	0.99 [Ω]	p	3 [-]
λ_m	0.0286 [V s]	$k_{3\lambda}$	3.7510^{-4} $[rpm]$

V. Simulations Results

Simulations of the proposed method have been analysed in Matlab-Simulink with the aid of the Xilinx System Generator toolbox in order to test the FPGA DT hysteresis controller and the proposed modulator in closed loop with the OEW-PMSM. The overall control structure implemented is presented in Fig. 8. The dc-link voltage is set to 540 V with the IGBT and SiC VSCs switching frequencies of 10 and 40 KHz respectively while the high speed starter-generator OEW-PMSM parameters are reported in Table IV. Fig. 9 shows the performances of the proposed SVPWM SZV instantaneous elimination without the DT hysteresis control. The third harmonic ZSC circulates due to the non-sinusoidal machine back EMF. The only ZSV is the one due to the DT distortion introduced on the 0-axis, in fact the ZSV ranges between $\pm\frac{V_{dc}}{3}$. In Fig. 10 the performances when the proposed DT hysteresis control is implemented on top of the SVPWM for instantaneous ZSV elimination are shown. The ZSV now assumes only values equal to $\pm\frac{V_{dc}}{3}$ corresponding to the voltage distortion introduced by the DT which are now controlled by compensating or not the DT. The possibility of controlling the hysteresis band is shown by stepping from 3 to 0 A band.

VI. Experimental results

The electrical and mechanical parameters of the OEW-PMSM used for the experimental validation have been estimated using the recursive least square method [20] and are reported in Table V. The machine used for the experimental validation is a scaled down version of the high speed machine of which discussed previously which therefore shows the same problems but on a smaller scale. The experimental set-up is composed by an OEW-PMSM coupled with a DC motor as shown in Fig. 11 while the control board specification can

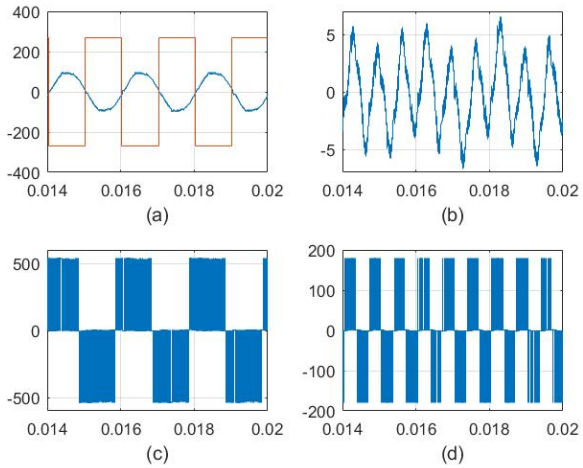

Fig. 9. Simulation Results for the proposed SVPWM for istantaneous ZSV elimination. 10000 rpm. (a) Phase current i_a. X-axis: 2ms/div; Y-axis: 200 A/div; V_{a0} (red line) X-axis: 2ms/div; Y-axis: 200 V/div.(b) ZSC i_0. X-axis: 2ms/div; Y-axis: 5 A/div (c) Phase voltage Vaa'. X-axis: 2ms/div; Y-axis: 500 V/div (d) ZSV V_0^{PMSM}. X-axis: 2ms/div; Y-axis: 100 V/div.

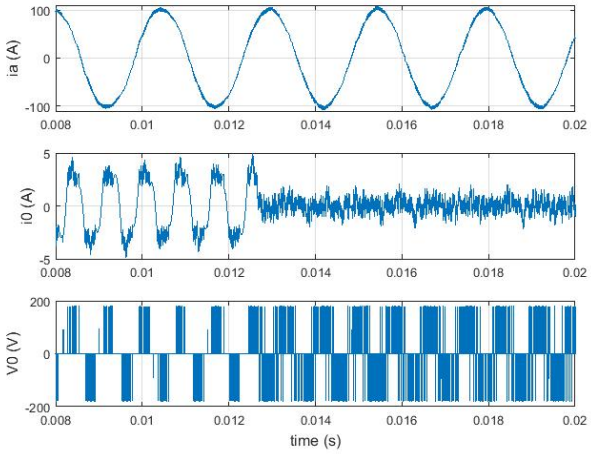

Fig. 10. Simulation Results for the proposed SVPWM and DT hysteresis control. Change of hysteresis band from 3 to 0 A. 8000 rpm. Top: phase current i_a; Middle: ZSC; Bottom: ZSV.

be found in [21]. The dc-link voltage is 80 V while the IGBT and SiC VSCs switching frequencies are 10 KHz and 40 KHz respectively. The IGBT DT is set to $3\mu s$ while the SiC one to $1\mu s$. The machine speed is set with a standard PI speed loop which feeds the reference q-axis current to the current loop. Fig. 12 shows the performances of the proposed modulation with the DT hysteresis band set to 0 A. The VSC A, i.e. the IGBT one is square wave modulated while the VSC B, i.e. the SiC one is modulated according to (2). The ZSC ripple is reduced by the modulation proposed while the third harmonic component has been eliminated by the DT hysteresis control. Fig. 13 shows the phase current profile and the ZSC for different values of the hysteresis band while Fig. 14 shows the phase currents and the ZSC when the hysteresis band is changed from 0.2 to 0.05 A. The hysteresis DT control is independent from the operating point of the

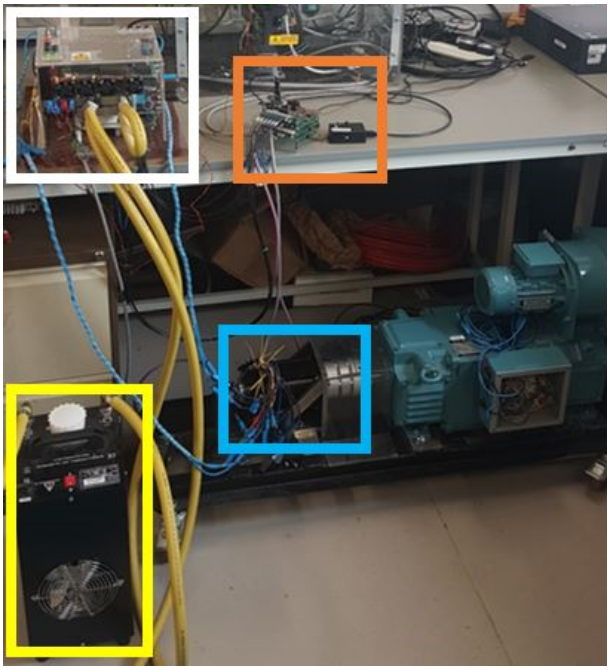

Fig. 11. Experimental set-up: Mixed technology IGBT-SiC common dc link conerter (white rectangle), control board (orange rectangle), chiller for liquid cooling of VSCs (yellow rectangle) and OEW-PMSM (blue rectangle).

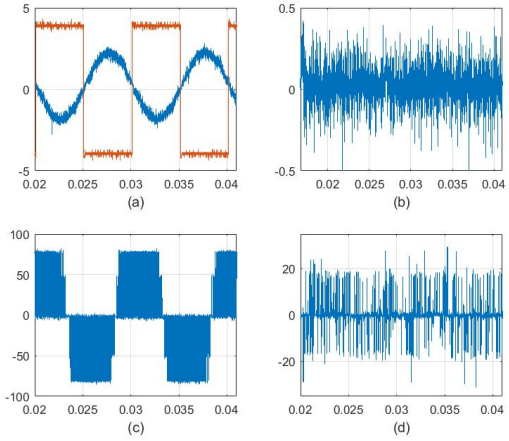

Fig. 12. Speed wm of 2000 rpm. Proposed modulation with DT hysteresis control and ZSC band set to 0 A. (a) Phase current i_a (blue line), V_{a0} (red line). X-axis: 5ms/div; Y-axis: 5 A/div (b) ZSC i_0. X-axis: 5ms/div; Y-axis: 0.5 A/div (c) Phase voltage Vaa'. X-axis: 5ms/div; Y-axis: 50 V/div (d) ZSV V_0^{PMSM}. X-axis: 5ms/div; Y-axis: 20 V/div

machine. Experimental results at 900 rpm with a load torque applied to the machine are shown in Fig. 15. In order to show the effectiveness of the proposed ZSC hysteresis controller over the whole speed range a speed transient from 0 to the rated speed of 3000 rpm has been performed as shown in Fig. 16. The ZSC hysteresis band is set to 0 except for the speed range that goes from 100 to 150 rad/s where it is set to 0.5 A. In this way it is possible to observe that the ZSC can be controlled in any speed range independently from the the operating point.

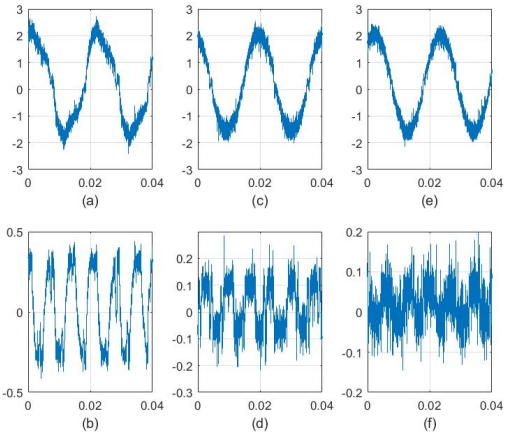

Fig. 13. Speed wm of 1000 rpm. Proposed modulation with DT hysteresis control for different values of ZSC band (a) Phase current i_a. X-axis: 20ms/div; Y-axis: 1 A/div (b) ZSC i_0, hysteresis band of 0.3 A. X-axis: 20ms/div; Y-axis: 0.5 A/div (c) Phase current i_a. X-axis: 20ms/div; Y-axis: 1 A/div (d) ZSC i_0, hysteresis band of 0.1 A. X-axis: 20ms/div; Y-axis: 0.1 A/div (e) Phase current i_a. X-axis: 20ms/div; Y-axis: 1 A/div (f) ZSC i_0, hysteresis band of 0.05 A. X-axis: 20ms/div; Y-axis: 0.1 A/div

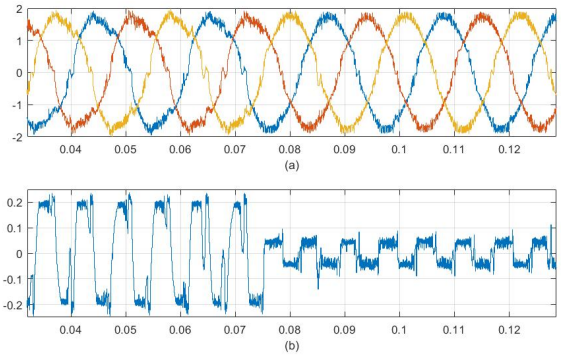

Fig. 14. Speed wm of 1000 rpm. Proposed modulation with DT hysteresis control. Change of the hysteresis band from 0.2 to 0.05 A (a) Phase currents. X-axis: 10ms/div; Y-axis: 1 A/div (b) ZSC i_0. X-axis: 10ms/div; Y-axis: 0.1 A/div

VII. Conclusions

In this paper an OEW-PMSM starter-generator fed by a dual-inverter with a common dc link has been considered. The effect of the VSCs' DT on the ZSV has been carried out. By combining the DT compensation method PBDTC with the modulation proposed in Part I an hysteresis control of the ZSC using the DT as a control action has been developed to suppress the ZSC flowing due to the non-sinusoidal back EMF. The different nature of the power modules used for the two converters, IGBT and SiC, has been exploited by square wave modulating the IGBT one in order to obtain higher system efficiency and reduce the ZSC circulating problem.

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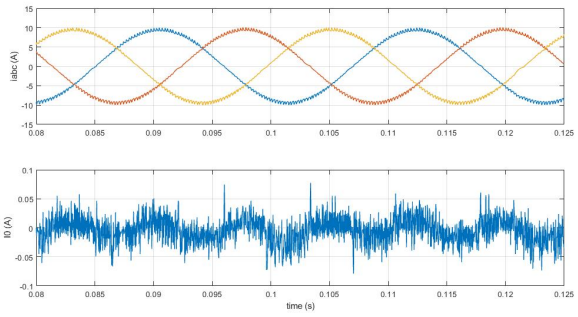

Fig. 15. Experimental results at wm of 900 rpm and increased load torque. Top: Phase current i_a, i_b, i_c (blue, red, and yellow respectively). Bottom: ZSC i_0.

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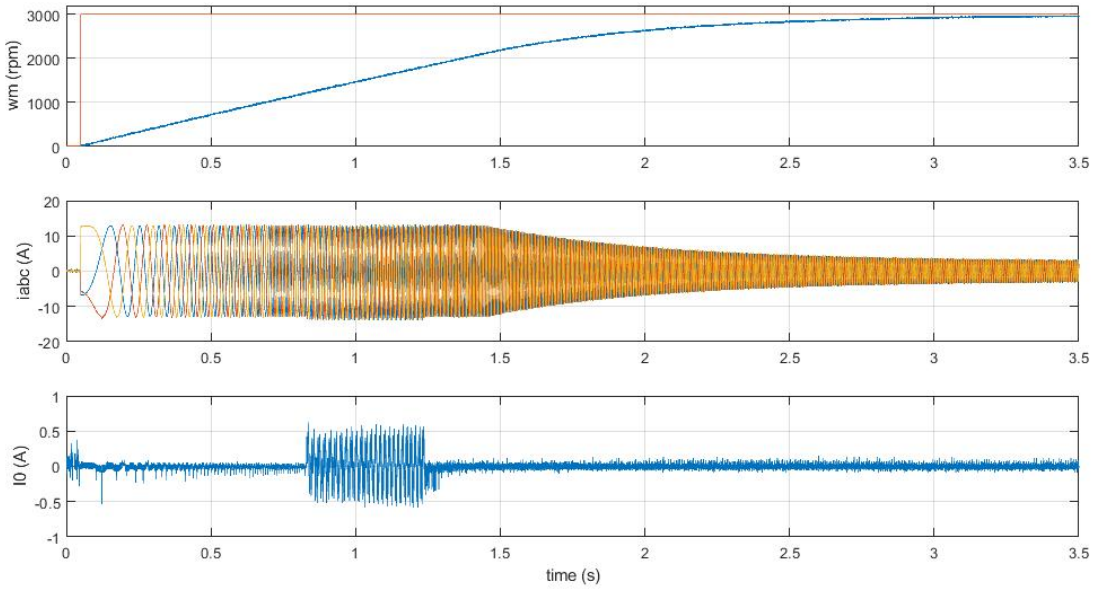

Fig. 16. Speed transient from 0 to 3000 rpm. Top: reference speed (red) and actual mechanical speed (blue). Middle: phase currents. Bottom: ZSC